Detector Support Group

We choose to do these things "not because they are easy, but because they are hard".

Weekly Report, 2021-09-01

Summary

Hall A – GEM

Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, Marc McMullen

- Populated one of two I^2C multiplexer boards for the gas flow sensors
- All GEM activity in the large cleanroom (EEL 124) is expected to be complete this week
    - ✶ SBS assembly and testing to be conducted in EEL 125

Hall A - Detectors

Brian Eng

- Developing Python script to control and monitor the high voltage of all detectors

Hall A – SoLID

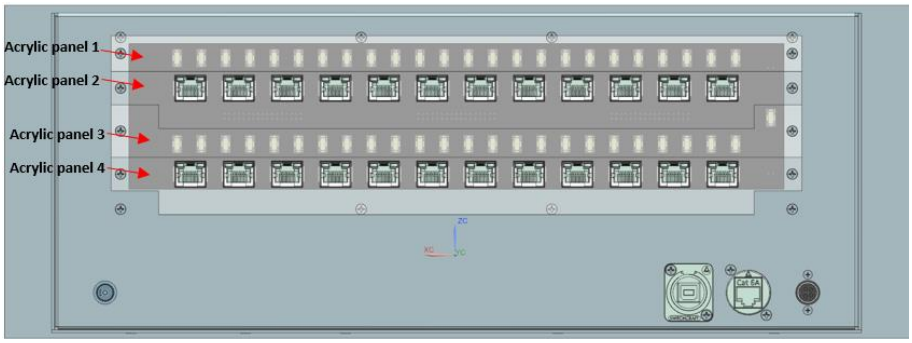
Mary Ann Antonioli, Pablo Campero, Brian Eng, Mindy Leffel, Marc McMullen

- Modified wiring to provide 24 and 5 VDC power required for the constant current source board (CCS) instrumentation
- Generated two Visio drawings of power distribution for CCS boards – actual and proposed
- Developing drawings: *Power Distribution Wiring Diagram*, *Power Supply Control Crate Connections*, and *PLC I/O, Remote A, Slot 1 Terminal Connections*
- Completed drawings: *Miscellaneous Instrumentation Wiring Diagram* and *Miscellaneous Instrumentation Cable Diagram*

Hall B – RICH-II

Mary Ann Antonioli, Peter Bonneau, Pablo Campero, Brian Eng, George Jacobs, Tyler Lemon, Marc McMullen

- Conducted, using Ansys, thermal analysis of RICH-II electronics panel
    - ✶ Calculated heat generated due to convection and conduction inside the panel
- Researching recovering source code of d0 test station's "ximea-shot" executable as INFN collaborators have not yet responded with source code
    - ✶ "ximea-shot" program acquires one image (or shot) from a Ximea CCD camera used to image the reflected point-source light off of a spherical mirror
    - ✶ Using Ghidra software, attempting to reverse engineer source code from executable; able to retrieve *some* elements
- Redesigned, using NX12, acrylic panel on back of hardware interlock chassis to make it easier to remove for maintenance
    - ✶ New panel design has four sections: two to cover fuses and two to cover RJ45 ports



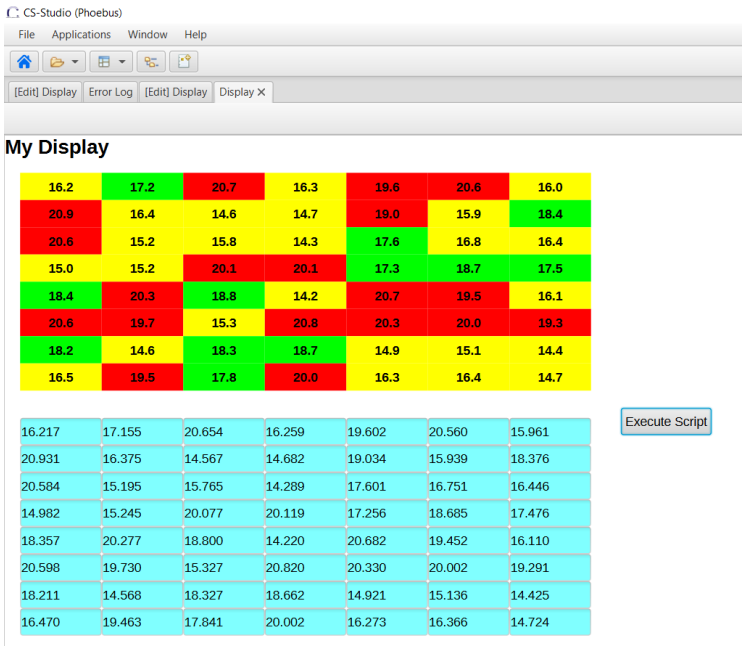
Rear of RICH-II hardware interlock chassis. Redesigned acrylic panel is shown as four parts covering fuses and RJ45 ports.

- Revising Backplane PCB – adding dedicated PCB connections for network cable shields

Hall C – NPS

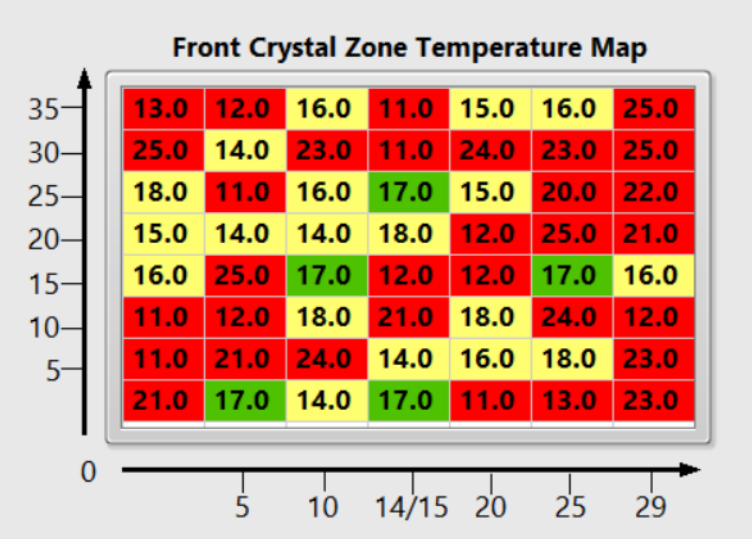
Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, Marc McMullen

- Calculated new expected current for HV Supply Cable testing taking into account both set voltage accuracy (±1% ± 1 V) and resistor accuracy (±1%)
- Developed, using Phoebus, first draft of EPICS Front Crystal Zone Temperature Map using local PVs and 56 random temperature values generated via an embedded JavaScript



Screenshot of EPICS Temperature Map screen developed using Phoebus

- Revised *Temperature Map* tab for LabVIEW Hardware Interlock Monitoring program
  - ✶ Temperature map now shows actual temperature for each sensor instead of average
  - ✶ Changed axes to reflect row and column numbers instead of crystal numbers



Screenshot of *Temperature Map* tab from the LabVIEW Hardware Interlock Monitoring program

EIC

Brian Eng

- Attended ECCE and ATHENA Tracking working group meetings
- Discussed Silicon installation procedure
    - ✶ May not have access to both ends of silicon tracker; checking to see if EMCal end cap can be removed in order to grant access to both ends

DSG – CAEN HV Test Stand

Mindy Leffel

- Terminated ground and high voltage wires on 24 of 48 cables